# COUNTER/FREQUENCY METER

S. S. AGARWAL AND P. S. Gill

CENTRAL SCIENTIFIC INSTRUMENTS ORGANIZATION, CHANDIGARH, INDIA

(*Received April* 20, 1966)

**ABSTRACT.** A transistorised digital frequency meter capable of operating up to 2 Mc/s has been described. The decade circuit uses 1–2–4–8 weighted working code and nor-transistor resistor logic system has been used for the decimal display.

The counter is the most reliable instrument for an accurate measurement of frequency, period, time interval, frequency ratio of the two applied signals and for the counting of regular or random electrical pulses. It could also be used for the measurement of non-electrical parameters by the use of suitable transducers

The counter consists of four main units.

(1) Input circuit which amplifies and shapes the incoming signal in order to present pulses of uniform amplitude and rise time to the succeeding circuit.

(2) The decades with display units which totalize the incoming counts and transform these into numerical display.

(3) The time base which consists of the crystal oscillator and decades, supplies the precisely known increment of time during which pulses are counted.

(4) Gate control which starts and stops the counting.

Fig. 1 shows the block diagram for frequency measurement. For other measurements mentioned above the same blocks are used but connected in a slightly different way.

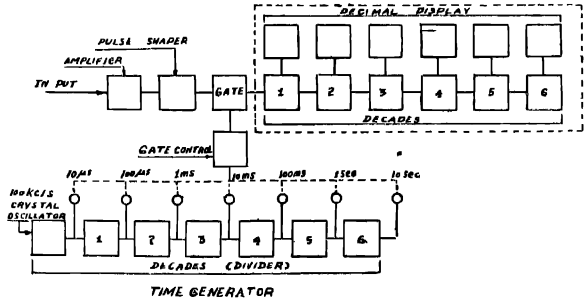


Fig. 1

An accurate measurement of frequency is made by counting the number of pulses for a precisely controlled time interval. The measurement of time or period is made by counting time base pulses for a period controlled by the incoming signal whereas frequency ratio is determined by counting the number of pulses of one signal for a period controlled by the other signal.

Technically, the most important section of a frequency meter is the decade and its associated display unit and these will be described here.

## DECADE UNIT

Basically, the decade circuit consists of four identical binary stages cascaded in series such that there would be one pulse in the output for every sixteen input pulses. However, the circuit has to be modified suitably in order that the scale of sixteen is reduced to a decade or scale of ten. Broadly speaking, this could be achieved by using either the feedback or the reset technique.

The feedback technique of modifying binary counts, although simple and economical, is not very satisfactory when operating at high frequencies. One reason is that the delay around the feedback loop and its associated decade must be less than the periodic time of the input signal. Secondly, any stage being supplied with feedback pulse in addition to some external input must be capable of resolving the two, in order that it shall not ignore the feedback pulse. These factors limit the operation of the circuit at high frequencies. These disadvantages are overcome by using the 'reset' technique.

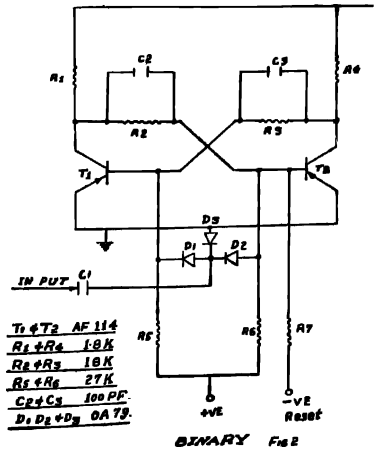


Fig. 2

The reset technique described here employs two Gate circuits such that the code of the resulting decade remains as for the pure binary 1-2-4-8 weighted working.

## GATE CIRCUIT

The technique used to modify the normal four-binary count of sixteen to ten is simply to allow the circut to count up to 9 in the normal fashion and make the 10th count reset the binaries into their starting condition. The count of 9 leaves the counter in the binary code condition 1001 and input pulse 10 would normally alter this to 1010. However, the change of state of the fourth binary on the eighth count closes gate $G_1$ and opens the gate $G_2$ so that when 10th pulse comes in, it changes over the condition of the fourth binary instead of the second, thus resetting the counter to 0000 condition.

These two gates $G_1$ and $G_2$ have been so arranged that when transistor $T_8$ is in saturation, gate $G_1$ is open and $G_2$ closed and vice versa when $T_8$ goes into cut cut off.

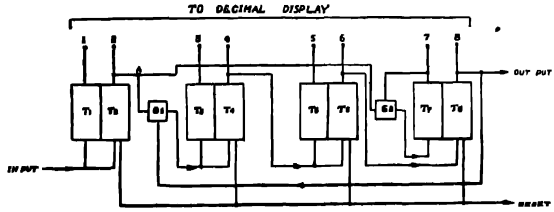


Fig. 3

## DECADE OPERATION

Consider Fig. 3. Initially the transistors $T_2$ $T_4$ $T_6$ and $T_8$ are in saturation and with each successive incoming pulse, the condition of these transistors is as shown in Table I.

Table 1 shows that all binaries behave conventionally up to 9 input pulses i.e. the incoming pulses at $A$ pass through gate $G_1$ to the second binary and do not pass through gate $G_2$ as it is closed, transistor $T_7$ being in cut-off condition. However, eighth input pulse changes the condition of binary 4, bringing transistor $T_7$ into saturation and $T_8$ into cut-off with the result that gate $G_1$ is closed and $G_2$ is open. Thus subsequent pulses at $A$ i.e. input pulse 10, will not affect the condition of binary 2 and instead directly changes the condition of the fourth binary, thus bringing transistors $T_2$ $T_4$ $T_6$ and $T_8$ in saturation, which is the condition for zero input. Hence zero condition appears once for every ten input pulses i.e. the system is a decade or scale of ten.

TABLE I

| | Binary I | | Binary II | | Binary III | | Binary IV | |
|---|---|---|---|---|---|---|---|---|
| Transistor No. → / Pulse No ↓ | $T_1$ | $T_2$ | $T_3$ | $T_4$ | $T_5$ | $T_6$ | $T_7$ | $T_8$ |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 2 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 3 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 4 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 5 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 6 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 8 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 9 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 10 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| Weights | 1 | | 2 | | 4 | | 8 | |

0 = Conduction (Saturation)
1 = Non Conducting (cut off)

The reset count switch enables the counter to be restored to its zero condition manually from any random setting When the switch is in the reset position, transistors $T_2$ $T_4$ $T_6$ and $T_8$ are brought into saturation by the application of external negative pulses to their bases thereby compelling the counter to adopt its zero condition.

## BINARY

Fig. 2 shows a conventional binary circuit capable of operating up to a counting speed of 2Mc/s reliably. The trigger differentiating circuit uses a diode $D_3$ instead of the conventional resistive load and diodes $D_1$ and $D_2$ serve the purpose of steering the trigger pulses to the appropriate points in the circuit

## DECIMAL DISPLAY

The information contained in a decade circuit can be transformed into a decimal display by various methods, the more popular being the use of meters responding to weighted currents and the use of diodes matrix system with Nixie tubes (for in-line readout) or with Neon indicators. In the circuit described

here, NOR transistor resistor logic system has been used with Neon indicators. This logic system by making use of resistors instead of diodes as in the diode matrix

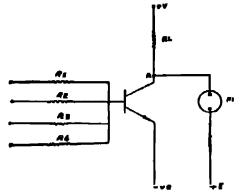

Fig. 4

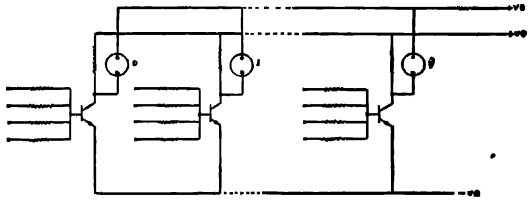

Fig. 5

system, makes it more economical and reliable, too, if the resistors are suitably chosen. This logic system can be used with Nixie tubes also.

Fig. 5 shows the circuit for the numerical display; complete circuit has, however, been shown for digits 0, 1 and 9. It uses ten NPN transistors for driving the ten Neon indicators.—one for each digit. The bases of these transistors are coupled to the collectors of the decade circuit through resistors in such a manner that only one transistor is turned on at a time which instantaneously corresponds

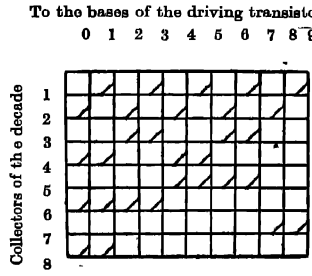


Fig. 6

to the number of counts stored in the decade. In normal fashion 40 coupling resistors have to be used i.e. four resistors for each digit. A few resistors have, however, been eliminated without in any way impairing the working of the circuit. This is shown in Fig. 6.

Let us now consider the operation of the circuit shown in Fig. 4 which is only for one digit. When the inputs of all the resistors are at '0' potential, corresponding transistors in the decade circuit are in saturation indicating the condition for the said digit. The driving transistor will then be turned on and the collector potential will fall towards zero so that the voltage applied across the Neon indicator will be $E$ volts which is sufficient to strike the neon indicators and the corresponding digit will light up. Now, if the input of even one of the resistors is at a negative potential, not all the corresponding transistors in the decade circuit are in saturation indicating that this is not the condition for the said digit. The driving transistor will therefore be cut off and the collector potential will rise towards supply voltage $V$ so that the voltage applied across the neon indicator will be $E$-$V$ volts which is not sufficient to strike the neon indicator and therefore the neon will not glow. In short, the circuit discussed can be considered as a gating circuit formed by four resistors followed by a transistor inverting amplifier.

## DESIGN CONSIDERATIONS

To ensure a satisfactory working of the circuit (Fig. 4) two conditions must be fulfilled.

1. When the inputs of all the resistors are at zero potential i.e. no input signal is applied, the transistor should be in saturation. To ensure this, the emitter is kept slightly negative.
2. When there is an input signal on any one of the resistors, the transistor should be in cut-off condition i.e. the amplitude of the input signal should be sufficient to bring the transistor into the said condition.

## CONCLUSION

The decimal display circuits described earlier (Scollar, 1965; Young, 1965) have used the conventional diode matrix system. T. D. Towers (1964) in his discussion has mentioned that there is hardly any standard cheap and reliable read-out device. The present discussion makes use of only thirty resistors logic system and as such it can be considered to be more economical and reliable. This system could also be used with decades having 1–2—2—4 and 1–2–4–2 code system. In addition, the circuit employed for the decade uses minimum number of components and operates satisfactorily up to 2 Mc/s with a minimum input signal of 100 mV peak.

ACKNOWLEDGMENT

The authors wish to express their thanks to Mr. B. P. Mital for his active help and work done in the design and development of the circuit throughout and also in the preparation of the manuscript.

REFERENCES

Barrow, C. W. M., 1964, *Electronic Engineering*, **36**, 660.
Scollar, I., 1965, *Electronic Engineering*, **37**, 468
Towers, T. D., 1964, *Wireless World*, **79**, 569.
Young, J. F., 1965, *Electronic Engineering*, **37**, 161.